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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/620,628
Filing Date: July 15, 2003
Appellant(s): ZHONG ET AL.

Jeanette Harms
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 10, 2006 appealing from the Office action mailed December 19, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

York, G. et. al., "An Integral environment for HDL verification" Verilog HDL Conference, 1995. Proceedings., 1995 International, IEEE (March 27, 1995), pp.9-18

Dawson, C., et al., "The Verilog procedural interface for the Verilog hardware description language" IEEE (1996), pp. 17-22

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1—2, 4, 6-7, 11-14, and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by York, G., et al., "An Integral environment for HDL Verification" (hereinafter referred to as York).

2. York was cited in a prior office action dated 7/30/02.

3. As for claim 1, York disclosed the invention as claimed, including a method for performing design verification [pg. 9, abstract], the method comprising:

specifying at least one hardware description language object that represents at lest one signal as a symbol in a design using a first statement that is part of a description language [pg. 12, section 3.1; pg. 14, section 3.3, pg. 12, fig. 2, module alu, output, where mode is symbolic expression, pg. 13, fig. 3, and pg. 14, section 3.3 fourth paragraph where the UART of fig. 3 is shown to inputs set to symbolic expressions: Note that the statements of the module description are part of "a description language"]; and

instructing a symbolic simulator in response to the first statement to treat the at least one description language object as a symbol [pg. 14, section 3.3, where the response to the description language objects, (the modules described in fig.'s 2 and 3) are symbolically simulated].

4. As for claim 11, York disclosed the invention as claimed, including an article of manufacture having at least one recordable medium having stored thereon executable instruction which, when executed by at least one processing device cause the at least one processing device to::

specify at least one hardware description language object that represents at lest one signal as a symbol in a design using a first statement that is part of a description language [pg. 12, section 3.1; pg. 14, section 3.3, pg. 12, fig. 2, module alu, output, where mode is symbolic expression, pg. 13, fig. 3, and pg. 14, section 3.3 fourth paragraph where the UART of fig. 3 is shown to inputs set to symbolic expressions: Note that the statements of the module description are part of "a description language"]; and

instructing a symbolic simulator in response to the first statement to treat the at least one description language object as a symbol [pg. 14, section 3.3, where the response to the description language objects, (the modules described in fig.'s 2 and 3) are symbolically simulated. Also note that York inherently disclosed and article of manufacture having at least one recordable medium having stored thereon executable instruction because the a computer program product having instruction which must be stored on a computer readable medium and be executed by a processing device in order to perform the functions of the function of verification as disclosed by York.].

5. As for claims 2, 4, 6, 12-14 and 16, York further disclosed
[claims 2 and 12] inserting the first statement into a design specification [fig. 2, see input, mode] and inputting the design specification into the symbolic simulator [pg. 14, section 3.3, first paragraph, lines 1-3, and paragraph four, lines 1-3, where the input is utilized by the symbolic simulator];
[claims 4 and 14] wherein the at least one description language object comprises a Verilog object [fig. 2];

[claims 6 and 16] wherein the at least one signal comprises an input [fig. 2, see input, mode];
[claims 7 and 17] specifying a check using a second statement, the check to perform a test to validate design functionality; and instructing the symbolic simulator using the second statement to perform the test [pg. 14, section 3.3, fourth paragraph: Note that the examiner interprets the use of the symbolic simulator to perform a check/test for verification to inherently include at least a statement that causes the simulator to do the checking, and therefore reads on a second statement as claimed]. HDL, Verilog, PLI [pg. 98, right hand side, lines 1-14, and also as cited in the rejection of claim 1].

6. As for claims 8 and 18, York further disclosed inserting the first and second statements into a design specification and instructing the symbolic simulator using the second statement to perform the test [see fig.'s 2 and 3, out and case, which signify the simulation with outputs to the variables out and state_reg, respectively; and pg. 14, section 3.3, especially 14, section 3.3, first paragraph, lines 1-3, and paragraph four, lines 1-3, where the input is utilized by the symbolic simulator].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9-10, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over York, G., et al., "An Integral environment for HDL Verification" (hereinafter referred to as York), in view of Dawson, Charles, et al., "The Verilog Procedural Interface for the Verilog hardware description language".

8. As for claims 9 and 19, York in view of Dawson disclose the invention substantially as claimed, including the method and apparatus for performing design verification as cited in the rejections of claims 1, 11, and 7-17.

York does not disclose that the second statement comprises a PLI.

Dawson discloses a PLI statement [pg. 17, PLI, pg. 18, left hand side, first full paragraph, pg. 21-22, section 4.2, the declaration of wire]. Dawson further discloses that the specifying the hardware declaration language object through the use of the first statement (VPI creation of the object) would be desirable [pg. 22, section 4.4 first paragraph].
Dawson discloses a second statement that is a PLI command [pg. 21, section 3.2].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of York and Dawson because having Dawson's second statement comprised of a PLI command would have improved York's system by requiring very little user interaction by automatically executing the simulation [see Dawson, pg. 21, section 3.2].

9. As for claims 10 and 20, York in view of Dawson discloses the invention substantially as claimed, including the method and apparatus for performing design verification as cited in the rejections of claims 1, 11, and 7-17.

York does not specifically disclose instructing the symbolic simulator to generate a file with information to locate an identified fault.

Dawson discloses instructing the symbolic simulator to generate a file with information to locate an identified fault [pg. 20, section 2.7].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of York and Dawson because having Dawson's symbolic simulator instructed to generate a file with information to locate an identified fault would have improved York's system by complementing the rest of the interface with the added ability to write files which provide valuable error information that could be useful to a designer for finding errors.

(10) Response to Argument

In the Appeal Brief, pages 6-10, applicant argues in substance:

A: York nor Dawson disclose specifying at least one hardware description language object that represents at least one signal as a symbol; and instructing a symbolic simulator in response to the first statement to treat the at least one hardware description language object as a symbol.

Examiner disagrees for the following reasons:

As to argument A: York discloses specifying at least one hardware description language object that represents at least one signal as a symbol; and instructing a symbolic simulator in response to the first statement to treat the at least one hardware description language object as a symbol [pages 12-15, figures 2 and 3, with particular attention to section 3.3 Symbolic Simulation – York discloses] specifying at least one

hardware description language object that represents at least one signal as a symbol on page 14, section 3.3 through the statements disclosing "The simulator includes symbolic simulation, which means that the user may set a node to a variable or expression instead of a particular logic value. A symbolic simulator extends this to propagate symbolic expressions over a set of variables, as well as simple values, and also Using the simulation capabilities of a symbolic simulator is much simpler. We start with the UART simulation, and set its test inputs to disable the scan path. Then we take verilog simulation, apply symbolic Boolean variables to the inputs of the receivers...and simulate symbolically. The circuit is initialized to the unknown X value, its inputs are set to symbolic Boolean variables, the circuit is simulated, and the combinational functions computed by the circuit appear on its output." Inputs, nodes, or variables are objects that are treated as symbols by the symbolic simulation. In order to describe the objects, a first statement into the simulator must be used. The symbolic simulator then takes a statement describing the objects. As symbols and treats it as a symbol via its representation of the object as an expression or Boolean variables such as those described at the bottom of page 14, under 1. "Such structures often use buses or multiplexers. For example, suppose we want to compute either (a + b) x c or (a x b) + c. depending on a control line." York's disclosure of symbolic simulation must use a programming statement in order to represent inputs as symbolic expressions or variables. Note on page 4 of the appeal brief, applicant expressly states that at "Specification, page 12, lines 13-14. The signals may be inputs, interrupts, memory values, or any other portion of a design that may be represented as an object in a

hardware description language." For the above reasons, examiner applies York's use of inputs (a description that is a hardware description language statement) and subsequent symbolic simulation (responding to the statement and representing the statement as a symbol through symbolic simulation) to meet the claimed limitations.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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